Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Claim 1 (previously presented): A one-time programming memory element, capable of being manufactured in a 0.13μm or below CMOS technology, comprising:

a capacitor having an oxide layer capable of passing direct gate tunneling current;

a write switch including a first switch transistor coupled between a first voltage and a first terminal of said capacitor and a second switch transistor coupled between a second voltage and a second terminal of said capacitor, said first and second switch transistors each having a gate oxide layer that is thicker than said capacitor oxide layer so as to have a voltage tolerance higher than that of said capacitor oxide layer, wherein closing said first and second switch transistors causes application of a voltage across said capacitor oxide layer; and

a read switch including plural transistors coupled to said capacitor, each read switch transistor having a gate oxide layer that is thicker than said capacitor oxide layer so as to have a voltage tolerance higher than that of said capacitor oxide layer;

wherein said capacitor is one-time programmable as an anti-fuse by application of said voltage across said capacitor oxide layer via said write switch transistors to cause direct gate tunneling current to rupture said capacitor oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.

Claim 2 (previously presented): The one-time programming memory element according to claim 1, wherein said capacitor oxide layer is approximately 20Å thick.

Claim 3 (previously presented): The one-time programming memory element according to claim 1, wherein said capacitor comprises a field effect transistor having source and drain regions coupled to ground, a gate coupled to said write switch and a gate dielectric forming said oxide layer.

Claim 4 (previously presented): The one-time programming memory element according to claim 3, wherein said field effect transistor has a deep N-well design including:

a P-well layer adjacent the source and drain regions;

a deep N-well layer below the P-well layer; and

a P-type substrate below the deep N-well layer.

Claim 5 (previously presented): The one-time programming memory element according to claim 1, wherein said write switch comprises a 5-volt tolerant switch of which said first and second switch transistors are 2.5-volt transistors with gate oxide layers that are thicker than said capacitor oxide layer, and wherein said voltage across said capacitor oxide layer is less than 7 volts.

Claim 6 (previously presented): The one-time programming memory element according to claim 1, further comprising a sensing circuit to sense whether said capacitor is programmed.

Claim 7 (previously presented): The one-time programming memory element according to claim 1, wherein a charge pump is not required to program said anti-fuse.

Claim 8 (previously presented): A process, compatible with 0.13μm or below CMOS technology, for making a one-time programming memory element, comprising the steps of:

forming a capacitor having an oxide layer capable of passing direct gate tunneling current;

forming a write switch including a first switch transistor coupled between a first voltage and a first terminal of said capacitor and a second switch transistor coupled between a second voltage and a second terminal of said capacitor, said first and second switch transistors each having a gate oxide layer that is thicker than said capacitor oxide layer so as to have a voltage tolerance higher than that of said capacitor oxide layer, wherein closing said first and second switch transistors causes application of a voltage across said capacitor oxide layer; and

forming a read switch including plural transistors each having a gate oxide layer that is thicker than said capacitor oxide layer so as to have a voltage tolerance higher than that of said capacitor oxide layer;

wherein said capacitor is one-time programmable as an anti-fuse, without a charge pump, by application of said voltage across said capacitor oxide layer via said write switch to cause direct gate tunneling current to rupture said capacitor oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.

Claim 9 (previously presented): The process according to claim 8, wherein said capacitor oxide layer is formed to a thickness of approximately 20Å thick.

Claim 10 (previously presented): The process according to claim 8, wherein said forming a capacitor step comprises forming a field effect transistor having source and drain regions coupled to ground, a gate coupled to said write switch and a gate dielectric forming said oxide layer.

Claim 11 (original): The process according to claim 10, wherein said forming a field effect transistor step further includes forming a deep N-well.

Claim 12 (currently amended): The process according to claim 8, wherein said forming write switch step comprises forming a 5-volt tolerance switch ~~switch~~ of which said first and second switch transistors are 2.5-volt transistors with gate oxide layers that are thicker than said capacitor oxide layer, and wherein said voltage across said capacitor oxide layer is less than 7 volts.

Claim 13 (original): The process according to claim 8, further comprising the step of forming a sensing circuit to sense whether said capacitor is programmed.

Claim 14 (original): The process according to claim 8, wherein said process does not require forming a charge pump to program said anti-fuse.

Claims 15-16 (previously cancelled)

Claim 17 (previously presented): The one-time programming element of claim 1, wherein said voltage applied across said capacitor oxide layer is less than 7 volts.

Claim 18 (previously presented): A one-time programming memory element, capable of being manufactured in a 0.13μm or below CMOS technology, comprising:

a capacitor having an oxide layer, approximately 20Å thick, capable of passing direct gate tunneling current;

a write switch including a first switch transistor coupled between a first voltage and a first terminal of said capacitor and a second switch transistor coupled between a second voltage and a second terminal of said capacitor, said first and second switch transistors each having a voltage tolerance higher than that of said capacitor, wherein closing said first and second switch transistors causes application of a voltage across said capacitor oxide layer; and

a read switch including plural transistors coupled to said capacitor, each read switch transistor having a voltage tolerance higher than that of said capacitor;

wherein said capacitor is one-time programmable as an anti-fuse by application of said voltage across said oxide layer via said write switch to cause direct gate tunneling current to rupture said oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.

Claim 19 (previously presented): A one-time programming memory element, capable of being manufactured in a 0.13μm or below CMOS technology, comprising:

a capacitor having an oxide layer capable of passing direct gate tunneling current;

a write switch including a first switch transistor coupled between a first voltage and a first terminal of said capacitor and a second switch transistor coupled between a second voltage and a second terminal of said capacitor, said first and second switch transistors each having a voltage tolerance higher than that of said capacitor, wherein closing said first and second switch transistors causes application of a voltage across said capacitor oxide layer; and

a read switch including plural transistors coupled to said capacitor, each read switch transistor having a voltage tolerance higher than that of said capacitor;

wherein said capacitor is one-time programmable as an anti-fuse by application of said voltage across said oxide layer via said write switch to rupture said oxide layer to form a conductive path having a resistance of approximately hundreds of ohms or less;

wherein said capacitor comprises a field effect transistor having source and drain regions coupled to ground, a gate coupled to said write switch and a gate dielectric forming said oxide layer; and

wherein said field effect transistor has a deep N-well design including:

a P-well layer adjacent the source and drain regions,

a deep N-well layer below the P-well layer, and

a P-type substrate below the deep N-well layer.

Claim 20 (previously presented): A one-time programming memory element capable of being manufactured in a 0.13μm or below CMOS technology, comprising:

a transistor configured as a capacitor and having an oxide layer capable of passing direct gate tunneling current;

a write circuit, including:

a first switch transistor connected between a first terminal of said capacitor and a first voltage, and

a second switch transistor connected between a second terminal of said capacitor opposing said first terminal and a second voltage; and

a read switch including plural transistors coupled to said capacitor;

wherein said capacitor is one-time programmable as an anti-fuse by application of a voltage, equal to a difference between said first and second voltages, across said oxide layer when said first and second switches are closed.

Claim 21 (previously presented): The one-time programming memory element of claim 20, wherein each of said first and second switch transistor has an oxide layer thicker than said capacitor oxide layer.

Claim 22 (previously presented): The one-time programming memory element of claim 1, wherein:

when said write switch transistors are closed and said read switch transistors are open, one-time programming occurs; and

when said read switch transistors are closed and said write switch transistors are open, reading occurs.